Step (a) of claims 21 and 24 has been amended to recite "forming a plurality of field insulating films in parallel with one another and perpendicular to a later formed plurality of word lines on a semiconductor substrate;" to clarify that the plurality of word lines are formed subsequent to the formation of the insulating films.

The Examiner is directed to page 13, lines 13 and 14 of the present application, where it is stated that "the field insulating films extend perpendicularly to word lines which will be formed later . . . ."

Step (c) in claims 21 and 24 has been amended to recite "forming a plurality of first polysilicon strips in parallel with one another perpendicularly to said plurality word lines;"

Step (e) in claims 21 and 24 has been amended to recite "patterning said second polysilicon layer, said second gate insulating film, and said plurality of first polysilicon strips to thereby form said plurality of word lines, each word line having a plurality of control gates and floating gates;"

The Examiner is directed to page 13, line 21 to page 14, line 2 of the present application, where it is stated that a first polysilicon layer (5a) is formed all over the first gate insulating film (4). The first polysilicon layer (5a) is then patterned into a plurality of layers 5a in parallel with each other. It can be seen from FIG. 10 in the present application that reference 5a refers to a plurality of polysilicon strips. Then a second gate insulating film 6 is formed all over the product. Portions of the second gate insulating film 6 formed outside a region where a memory cell array is to be formed are then removed. Thereafter, a second polysilicon layer 7a is formed all over the second gate insulating film 6. Subsequently, the second polysilicon layer 7a, the second gate insulating film 6, and the first polysilicon layer (5a) are patterned to form control gates and floating gates of a wordline. (See page 14, lines 8-28 and FIG. 11B).

The Applicant believes that claims 21 and 24 now fully comply with 35 U.S.C. 112, second paragraph.

In paragraph 4 of the outstanding Office Action, the Examiner states that claim 21 recites the limitation "said top portion of the plurality of the bit studs" and "said

bottom portion of the plurality of the bit studs" in the last line of the claim. The Examiner states that there is insufficient antecedent basis for this limitation in the claim.

The last line of claim 21 has been amended to recite "wherein said bottom portion of said bit line is connected to a top portion of said plurality of bit studs and a bottom portion of said plurality of bit studs is connected to said drain regions."

In paragraph 6 of the outstanding Office Action, claims 21, 22, and 24 stand rejected under 35 U.S.C. 103(a) as unpatentable over Kamiya, et al. (U.S. Patent No. 5,838,615) in view of Kim (U.S. Patent No. 5,834,807).

The rejection is respectfully traversed.

Applicant incorporates by reference the various arguments set forth in the prior amendment filed April 19, 2001 to the extent that the Examiner has repeated the same grounds of rejection as set forth in the prior office action (January 4, 2001). By way of the instant amendment, the Applicant makes the following additional arguments.

Regarding amended claim 21, the present invention as recited in amended claim 21 is reduced to practice after a memory transistor has been fabricated. In brief, amended claim 21 includes the steps of covering a substrate with a first interlayer insulating film; forming contact holes only above both drain and source diffusion layers; forming a common source line of a first wiring layer through the contact holes to thereby form a region which will partially form a bit line only through the contact holes formed in the drain regions; covering a resultant product with a second interlayer insulating film; forming a through-hole just above the region; and forming a bit line of a second wiring layer.

The invention recited in amended claim 21 is structurally distinguishable from Kamiya as follows:

(a) In preferred embodiments of the invention, contact holes (11) are formed through the first interlayer insulating film (10) only above the drain and source diffusion

layers (8a and 8b) in all memory cell transistors. Each of the contact holes has an area smaller than an area of each of the diffusion layers.

(b) In preferred embodiments of the invention, the first metal wiring layer is designed so that it does not make contact with either the field insulating films (3) or the sidewall spacer (9).

(c) In preferred embodiments of the invention, the first metal wiring layer fills the contact holes formed in the drain and source diffusion layers, is located above a surface of the first interlayer insulating film, and has a width greater than a diameter of the contact hole. The common source line (12a) formed of the first metal wiring layer extends in parallel with a field insulating film (3). Raised portions are formed in the first metal wiring layer only above the contact hole formed in source regions of the memory cells, to thereby define the bit line. The first metal wiring layer is formed as an island above the contact holes formed in the drain regions.

The above-mentioned features, which are distinguishable over Kamiya, provide the following advantages:

The advantage of the distinguishing feature described in (a) is as follows:

Because the contact holes which are formed over both the drain and source regions have the same dimensions, for example the same diameter, variance in fabrication conditions which may be harmful, such as exposure and registration margin, are avoided by embodiments of the invention.

In contrast, the contact hole 113 and the slit 114 taught by Kamiya have different shapes from each other. Accordingly, variance in fabrication conditions which may be harmful, such as exposure and registration margin, may result in poor fabrication margin and reduction in fabrication yield.

The present invention thus has advantages over the device taught by Kamiya.

The advantage of the distinguishing feature described in (b) is as follows:

In general, when data is written into or is erased from a non-volatile memory such as a flash memory, a high voltage is applied to both a source and a drain. Because the wiring layer in the device taught by Kamiya makes contact with the field insulating film, such devices might be inadequately insulated from one another electrically. In particular, since the field insulating film makes contact at its end, that is, at its thinnest portion to the wiring layer (see reference numerals "101" and "109" in FIG. 7 in Kamiya), it would be impossible in the device taught by Kamiya to reduce a space between adjacent devices, resulting in difficulty in reducing a size of a memory cell.

In the device taught by Kamiya, the first wiring layer makes contact with the sidewall spacer. When a contact hole is formed through the tungsten film 115, the sidewall spacer is exposed to etching, resulting in no protection to a sidewall of a memory cell transistor. This may result in a reduction in the amount of electric charge maintained by the non-volatile memory, which characteristic is the most salient feature of a non-volatile memory.

The present invention thus has advantages over the device taught by Kamiya.

The advantage of the distinguishing feature described in (c) is as follows:

In the present invention, since the first metal wiring layer is formed above a surface of the first interlayer insulating film and has a width greater than the diameter of the contact hole, misregistration may be avoided when a through-hole is formed therethrough.

The common source line formed of the first metal wiring layer is formed on the field insulating film in parallel with the field insulating film, and the first metal wiring layer is designed to have a raised portion only on the contact hole formed in a drain region of a memory cell for making electrical contact with the contact, to thereby form a bit line. This ensures a higher density in arrangement of devices and reduction in a size of a memory cell.

The Examiner states that it is obvious in view of Kim that the second wiring layer is located on the second interlayer insulating film. In the device taught by Kim, the sidewall spacer 62 and the insulating film 52 are formed to attempt to provide the same function as the first interlayer insulating film of the present invention. However, Kim cannot provide the same functions as those of the present invention, unless both the first and second insulating films cover the product.

Thus, for the reasons stated above, the subject matter of Applicants' invention as a whole would not have been obvious at the time the invention was made to a person having ordinary skill in the art. Thus, the Patent and Trademark Office has not made out a *prima facie* case of obviousness under the provisions of 35 U.S.C. 103(a) and amended claim 21 is believed to be allowable.

Regarding claim 22, because amended claim 21 is believed to be allowable, claim 22, which depends from amended claim 21, is also believed to be allowable.

Regarding amended claim 24, the same arguments as those made above with respect to amended claim 21 may be made with respect to claim 24, since the bit line and the common source line are interchanged between claims 21 and 24.

In particular, amended claim 24 provides the advantage that a memory cell gate can be backed with the second metal wiring layer without an increase in a size of a memory cell.

Thus, for the reasons stated above, the subject matter of Applicants' invention as a whole would not have been obvious at the time the invention was made to a person having ordinary skill in the art. Thus, the Patent and Trademark Office has not made out a *prima facie* case of obviousness under the provisions of 35 U.S.C. 103(a) and amended claim 24 is believed to be allowable.

In paragraph 7 of the outstanding Office Action claim 23 stands rejected under 35 U.S.C. 103(a) as unpatentable over Kamiya, in view of Kim, as applied to claim 21, and in further view of Yonemoto (U.S. Patent No. 5,506,434).

In paragraph 7 of the outstanding Office Action claim 23 stands rejected under 35 U.S.C. 103(a) as unpatentable over Kamiya, in view of Kim, as applied to claim 21, and in further view of Yonemoto (U.S. Patent No. 5,506,434).

The rejection is respectfully traversed.

Regarding claim 23, because amended claim 21 is believed to be allowable, claim 23, which depends from amended claim 21, is also believed to be allowable.

In paragraph 8 of the outstanding Office Action claims 25 and 26 stand rejected under 35 U.S.C. 103(a) as unpatentable over Kamiya, in view of Kim, as applied to claim 24, and in further view of Cacharelis, et al. (U.S. Patent No. 5,550,072) (hereinafter Cacharelis).

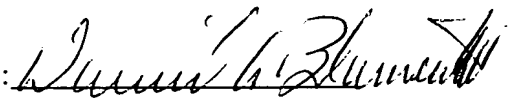
The rejection is respectfully traversed.

Regarding claims 25 and 26, because amended claim 24 is believed to be allowable, claims 25 and 26, which depend directly or indirectly from amended claim 24, are also believed to be allowable.

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance. Reexamination and reconsideration of the application, as amended, and allowance of the claims at an early date is respectfully requested.

Respectfully submitted,

Dated: November 1, 2001

By: 

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Takaaki NAGAI et al.

Title: EEPROM SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

Appl. No.: 09/606,159

Filing Date: 06/29/2000

Examiner: P. Brock, II

Art Unit: 2815

MARK-UP VERSION OF AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action mailed May 11, 2001, please amend the above-identified application as follows:

IN THE CLAIMS:

Please enter the following amended claims:

21. (Twice Amended) A method of fabricating an EEPROM semiconductor device having a plurality of memory cell transistors, comprising the steps of:

(a) forming a plurality of field insulating films in parallel with one another and perpendicular to a later formed plurality of word lines on a semiconductor substrate;

(b) forming a first gate insulating film in each of active regions;

(c) forming a plurality of first polysilicon ~~layers~~strips in parallel with one another perpendicularly to said plurality of word lines;

(d) forming a second gate insulating film and a second polysilicon layer all over the product resulting from said step (c);

(e) patterning said second polysilicon layer, said second gate insulating film, and said plurality of first polysilicon ~~layer~~ strips to thereby form said plurality of word lines, each word line having a plurality of ~~a~~ control gates and ~~a~~ floating gates;

(f) forming drain and source regions;

(g) forming a first interlayer insulating layer all over the product resulting from said step (f);

(g') forming contact-holes through said first interlayer insulating layer only above both said drain and source regions in said plurality of memory cell transistors;

(h) forming a first metal wiring layer which is patterned so as to form both a common source line extending in parallel with said plurality of word lines and connecting source regions to one another and a plurality of bit studs extending to said drain regions~~;~~, said first metal wiring layer being formed above a surface of said first interlayer insulating layer;

(i) forming a second interlayer insulating layer all over the product resulting from said step (h); and

(j) forming a second metal wiring layer which is patterned so as to form a bit line extending perpendicularly to said plurality of word lines and connecting said drain regions with each other, said bit line having a top portion and a bottom portion with said top portion being wider than said bottom portion,

wherein said bottom portion of said bit line is connected to ~~said~~ a top portion of said plurality of bit studs and ~~said~~ a bottom portion of said plurality of bit studs is connected to said drain regions.

24. (Twice Amended) A method of fabricating an EEPROM semiconductor device having a plurality of memory cell transistors, comprising the steps of:

(a) forming a plurality of field insulating films in parallel with one another and

perpendicular to a later formed plurality of word lines on a semiconductor substrate;

(b) forming a first gate insulating film in each of active regions;

(c) forming a plurality of first polysilicon ~~layers~~strips in parallel with one another perpendicularly to said plurality of word lines;

(d) forming a second gate insulating film and a second polysilicon layer all over the product resulting from said step (c);

(e) patterning said second polysilicon layer, said second gate insulating film, and said plurality of first polysilicon ~~layer~~ strips to thereby form said plurality of word lines, each word line having a plurality of ~~a~~ control gates and ~~a~~ floating gates;

(f) forming drain and source regions;

(g) forming a first interlayer insulating layer all over the product resulting from said step (f);

(g') forming contact-holes through said first interlayer insulating layer only above both said drain and source regions in said plurality of memory cell transistors;

(h) forming a first metal wiring layer which is patterned so as to form both a bit line connecting said drain regions to one another, and a plurality of source studs extending in parallel with said plurality of word lines, said plurality of source studs connecting to said source regions, said plurality of source studs having a top portion and a bottom portion with said top portion of said plurality of source studs~~;~~, said first metal wiring layer being formed above a surface of said first interlayer insulating layer;

(i) forming a second interlayer insulating layer all over the product resulting from said step (h); and

(j) forming a second metal wiring layer which is patterned so as to form a common source line connecting said source regions with each other, said common source line having a top portion and a bottom portion with said top portion of said common source line being wider than said bottom portion of said common source line,

wherein said bottom portion of said common source line is connected to said top portion of said plurality of source studs and said bottom portion of said plurality of source studs is connected to said source regions.